



FSMC-01-1507

December 10, 2003

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/661,745 09/14/03 |

Chia-Ta Hsieh

A TRAPEZOID FLOATING GATE TO
IMPROVE PROGRAM AND ERASE SPEED
FOR SPLIT GATE FLASH

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on December 19, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

S.B.A. 12/19/03

U.S. Patent 5,723,371 to Seo et al., "Method for Fabricating a Thin Film Transistor Having a Taper-Etched Semiconductor Film," teaches a method for fabricating a thin film transistor having a taper-etched semiconductor film, where the sharpness of corners is reduced.

U.S. Patent 5,728,259 to Suzawa et al., "Process for Fabricating Thin-Film Semiconductor Device Without Plasma Induced Damage," discloses a process for tapered silicon films in a method of fabricating a semiconductor device in which a gate insulating layer has no plasma induced damage.

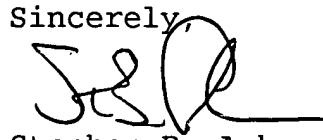
U.S. Patent 6,228,695 to Hsieh et al., "Method to Fabricate Split-Gate with Self-Aligned Source and Self-Aligned Floating Gate to Control Gate," discloses a split-gate flash memory cell with self-aligned source and self-aligned floating gate to control gate.

U.S. Patent 6,259,131 to Sung et al., "Poly Tip and Self Aligned Source for Split-Gate Flash Cell," discloses a method of forming a polysilicon gate tip in split-gate flash memory cells for enhanced F-N tunneling.

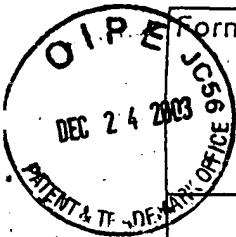
TSMC-01-1507

U.S. Patent 5,393,682 to Liu, "Method of Making Tapered Poly Profile for TFT Device Manufacturing," discloses a method for making tapered polysilicon gates.

Sincerely,

A handwritten signature in black ink, appearing to read "SBA".

Stephen B. Ackerman,
Reg. No. 37761



~~Form PTO-1449~~

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Doctor Number (Optional)

American Standard

TSMC-01-1507

(0/661,745

Applicant: John T. Hinkle

King Date

Filing Date 09/12/03

Draw a line

U. S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSMISSION
						YES
						NO

OTHER DOCUMENTS (including Author, Title, Date, Portion or Page, Etc.)

Examiner

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.